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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/314,750	05/19/1999	HIROSHI MURAKAMI	0941.63081	5601

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EXAMINER	
LESPERANCE, JEAN E	

ART UNIT	PAPER NUMBER
2674	22

DATE MAILED: 04/13/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/314,750	MURAKAMI, HIROSHI	
	Examiner	Art Unit	
	Jean E Lesperance	2674	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 December 2003*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 May 1999* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

ETAILED ACTION

Drawings

This application has been filed with informal drawings which are acceptable for examination purposes only. Formal drawings will be required when the application is allowed.

Claim Rejections - 35 U. S. C § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 2-11 are rejected under 35 U. S. C. 102 (e) as being unpatentable over U. S. Patent # 5,815,136 ("Ikeda et al.").

As for claims 2, 6, and 7, Ikeda et al. teach a liquid crystal panel Fig. 16 (132) corresponding to a display unit; the data bus Fig. 16 (102) corresponding to a display data line which supplies data of the image from an exterior of said display unit; the CPU Fig. 16 (1601) which may include a lot of memories which is different from the main memory Fig. 16 (1602) corresponding to memories which store information for controlling displaying of the data of the image on said display unit said

information being different from said data image; the timing control circuit Fig. 16 (1610) corresponding to an operation circuit unit which controls said display unit to display the data of the image supplied through said display data line based on the information stored in said memories; a data bus which exterior to said display device Fig. 16 (1605) corresponding to the data bus which connects said memories to an exterior of said display device and supplies the information to said memories from the exterior of said display device; and an address bus which is exterior to said display device Fig. 16 (1604) corresponding to an address bus which connects said memories to the exterior of said display device, and supplies address signals for selecting one of said memories; a scanning circuit Fig. 16 (130) controls by the timing control which is controlled by the CPU (memories) corresponding to a gate driver which drives the gate lines; a driver Fig. 16 (105-1) controls by the timing control which is controlled by the CPU (memories) corresponding to the data driver.

As for claim 3, Ikeda et al. teach a shift register Fig.2 (205-1) corresponding to the gate and data drivers include a shift register.

As for claim 4, Ikeda et al. teach a decoder Fig. 18A (118-2) corresponding to the gate and data drivers include a decoder.

As for claim 5, Ikeda et al. teach a address counter Fig. 29A (155) corresponding to the gate and data drivers include an address counter.

As for claim 8, Ikeda et al. teach the address converter of each of said driver circuit elements converts the address given from said external device into an address of the display memory of that driver circuit element on the basis of said

driver identification information indicative of that driver circuit element (column 42, lines 59-64) corresponding to a display-information acquisition circuit which acquires information about said display unit; the CPU Fig. 16 (1601) which may include a lot of memories which is different from the main memory Fig. 16 (1602) corresponding to display-information memories which store the information about said display unit.

As for claim 9, Ikeda et al. teach if the display operation is not performed at the fixed period, the quality of display of the liquid crystal panel is deteriorated. In the present embodiment, the two stages of latch circuits 187 and 189 are provided for enabling the display operation at the fixed period even in the case where the updating access and the display access overlap (column 30, lines 26-32) corresponding to a display-information acquisition circuit checks said display unit to acquire information about said display unit with regard to a defect of said display unit.

As for claim 10, Ikeda et al. teach the address converter of each of said driver circuit elements converts the address given from said external device into an address of the display memory of that driver circuit element on the basis of said driver identification information indicative of that driver circuit element (column 42, lines 59-64) corresponding to said display data acquisition circuit acquires the information about the said display.

As for claim 11, Ikeda et al. teach the data lines 136 and the scanning lines 137 are arranged in a matrix form so that 320.times.240 pixels are formed at the

intersections of the lines 136 and 137 (column 10, lines 6-8) corresponding to a plurality of pixel electrodes corresponding to the respective polysilicon thin film transistor. It is well know in the art to have a polysilicon thin film transistor.

Response to Amendment

Applicant's arguments filed 12-5-2003 have been fully considered but they are not persuasive. The applicant argued that the prior art, Ikeda, teaches clearly that the information in the CPU 1601 is the same as the information in the memory 1602. Ikeda disagrees with the applicant because Ikeda teaches that the driver memory map when seen from the liquid crystal drivers 105-1 and 105-2 is different from the screen memory map when seen from the CPU 1601 (column 14, lines 31-33) which is contrary to the applicant statement above. The applicant argued that either the main memory 1602 or the CPU 1601 actually includes memories, which store information for controlling the display of data. Examiner disagrees with the applicant here because the prior art, Ikeda, teaches numeral 1609 denotes a buffer for display data. At Figure 16 of the prior art, you can see that buffer 1609 receives information directly from the CPU, which means that the CPU includes memories, which store information for controlling the display data. The applicant argued that the prior art does not teach a signal from the control signal bus 1606 is based on information stored in the CPU 1601 or the main memory 1602. Examiner disagrees with the applicant again because the information that are going in the control signal bus are information that are received from the CPU or the main memory to execute certain commands for the column driver of the liquid

crystal display (132). The applicant argued that the prior art does not teach that both the data bus and address bus connect the display control information memories to the exterior of the display to control the device. The examiner disagrees the applicant because if you look at Figure 16, the data bus and the address bus are not included in the control signal bus, which control the system. The applicant argued that nowhere does the prior art teach that display control information is transmitted through the address bus or that the display control information memories may be selected according to the address signals supplied through the address bus. Examiner disagrees with the applicant again because the display control information is inherently transmitted through address bus. The claims are so broad and vague in the way they are written. The applicant has to amend the claims to be more specific and clear of the real invention in order to overcome the rejection. Therefore, the rejection is maintained.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jean Lesperance whose telephone number is (703) 308-6413. The examiner can normally be reached on from Monday to Friday between 8:OOAM and 4:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Hjerpe, can be reached on (703) 305-4709 .

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to:

(703) 872-9314 (for Technology Center 2600 only)

Hand-delivered responses should be brought to Crystal Park 11, 2121 Crystal drive, Arlington, VA, Sixth Floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the technology Center 2600 Customer Service Office whose telephone number is (703) 306-0377.

Jean Lesperance

Art unit 2674

Date 4-6-2004

RICHARD HJERPE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600